



## “ROC” Chips Readout

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# Presentation of the “ROC” Chips Readout

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## Abstract

The OMEGA group at LAL has designed 3 chips for ILC calorimeters: one analog (SPIROC) and one digital (HARDROC) for the hadronic one and also one for the electromagnetic one (SKIROC). The readout and the management of these different chips will be explained.

To minimize the lines between the ASICs and the DAQ, the readout is made thanks to 2 lines which are common for all the chips: Data and TransmitOn. As the chips are daisy chained, each chip is talking to the DAQ one after the other. When one chip has finished its readout, it starts the readout of the chip just after. Moreover, during this readout, only the chip which is talking to the DAQ is powered: this is made thanks to the POD (Power On Digital) module in the ASIC. In the ILC mode, readout sequence is active during inter bunch crossing (like ADC conversion).

Another chip designed for PMM2 R&D program (PARISROC) integrates a new selective readout: that's mean only hit channels are sent to the DAQ in a complete autonomous mode.

## I. GENERAL OVERVIEW

### A. Some ROC chips and their applications

#### 1) MAROC:

MAROC (Multi-Anode ReadOut Chip) is designed to read multi-anode photomultipliers [1] of the ATLAS luminometer made of Roman pots (Figure 1).

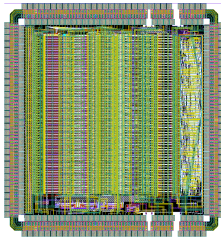


Figure 1: MAROC chip layout

#### 2) SKIROC:

SKIROC (Silikon Kalorimeter ReadOut Chip) has been designed to read-out the upcoming generation of Si-W calorimeter featuring ILC requirements (Figure 2).

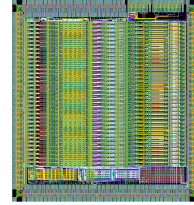


Figure 2: SKIROC chip layout

#### 3) HARDROC:

HARDROC (HADronic Rpc Detector ReadOut Chip) is the front end chip [2] designed for the readout of the RPC or GEM foreseen for the Digital HADronic CALorimeter of the future ILC (Figure 3).

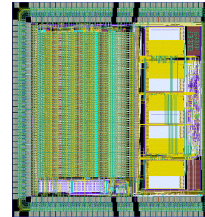


Figure 3: HARDROC chip layout

#### 4) SPIROC:

SPIROC (Silicon Photomultiplier Integrated ReadOut Chip) is a dedicated front-end electronics [3] for an ILC prototype of hadronic calorimeter with Silicon photomultiplier readout (Figure 4).

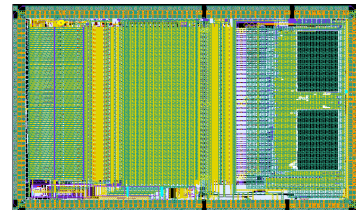


Figure 4: SPIROC chip layout

#### 5) PARISROC:

PARISROC (Photomultiplier ARray Integrated in Sige ReadOut Chip) is the front end ASIC designed for the PMM2 R&D project dedicated to neutrino experiments (Figure 5).

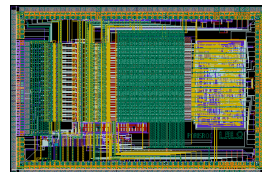


Figure 5: PARISROC chip layout

## B. High level working

The ROC chips can be divided in 2 groups: analog and digital ones. It depends if the signal from the detector is first stored into an analog way or directly in a digital way.

For analog chips, discriminated analog signals are first stored into an analog memory (the SCA: switched capacitor array) and then converted into digital words thanks to an ADC. These digital values are stored in a RAM to be readout at the end of the acquisition cycle.

For digital chips, the ADC is not needed as data are directly saved into the RAM. This is shown in next Figure 6.

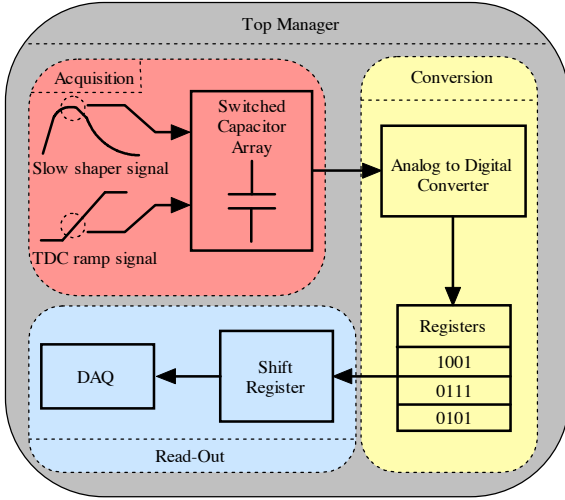


Figure 6: High level working

## C. Main analog block

These analog chips are based on Switched Capacitor Array (SCA). The number of channels managed can be up to 64. Fine time measurement is available depending on the application and experiment. The main architecture of analog part is given below in Figure 7.

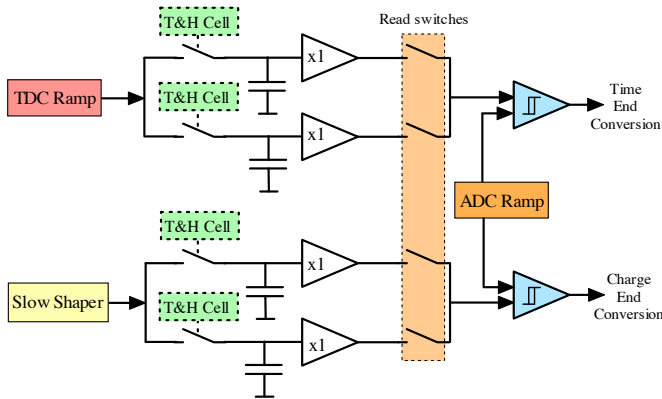


Figure 7: Main analog block

Figure 8 is an example of the behaviour of a “Track & Hold Cell” which allows to lock the capacitor value at the maximum of the analog signal.

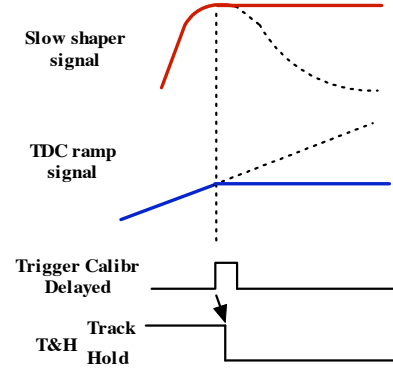


Figure 8: Behaviour of Track and Hold cell

## II. TIMING CONSIDERATIONS

### A. Global overview

Depending on the application, acquisition module is not active all the time. For example, in bunch crossing train sequence like in the future ILC, acquisition is stopped after each train (Figure 9). This is the case for SKIROC, SPIROC and HARDROC chips for ILC calorimeters.

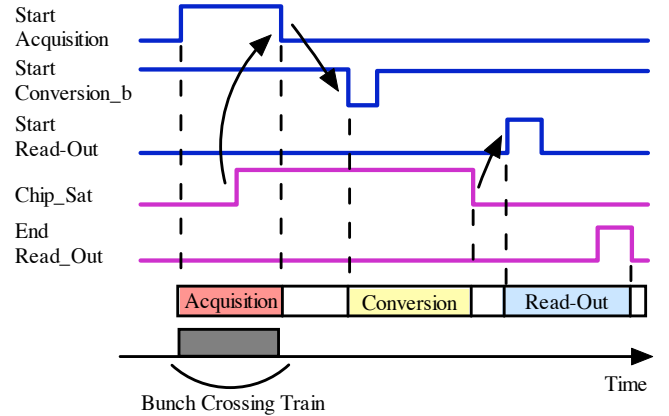


Figure 9: ILC sequences

In neutrino experiment, acquisition is never stopped. This is the case for PARISROC chip which can handle an acquisition active all the time. During its conversion and readout phases, discriminated analog signals can be stored in the SCA if it is not full.

### B. Future ILC requirements

Future ILC is based on a 200ms bunch crossing train period (Figure 10). For the front end electronics, the digital part of acquisition is active only during the bunch crossing and the conversion and the readout are active during inter bunch crossing.

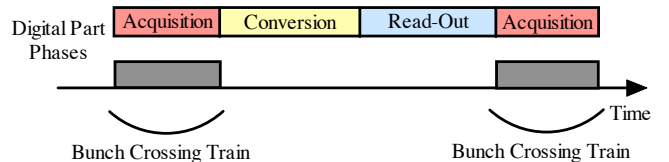


Figure 10: ILC timing requirements



### 1) Acquisition and conversion phases

PowerON is set during the reset phase before each acquisition. It allows to start the LVDS receiver and consequently the clocks. When clocks are established, reset can be released; this is done after reset startup time which is about 200 ns. That's why reset duration must be longer than LVDS wakeup time (Figure 14).

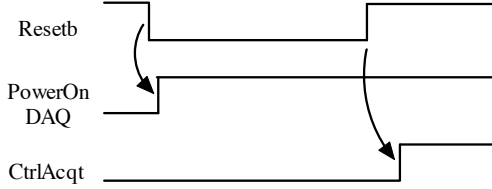


Figure 14: Start of acquisition

PowerON is released at the end of the conversion. It is synchronized internally to properly stop the clocks. Effective PowerOn release is done after few clock ticks (Figure 15).

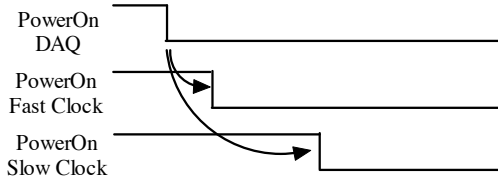


Figure 15: Stop of acquisition and conversion

PowerON is asynchronously set by the DAQ during the reset state and it is synchronously released by the POD in each chips.

### 2) Readout phase

PowerON during daisy chained readout is done by the previous chip thanks to its calibrated EndReadout which is the StartReadout of the chip just after it. This signal allows to start LVDS receiver and then synchronously the clocks. Finally, it generates an internal StartReadout for state machines (Figure 16).

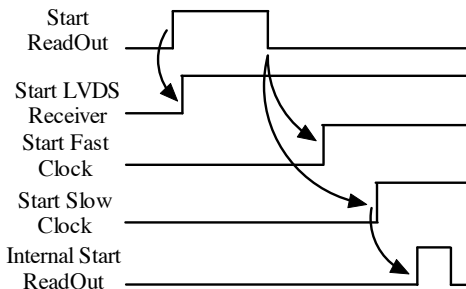


Figure 16: Start of readout

At the end of the readout, clocks and LVDS receivers are stopped synchronously (Figure 17). Effective PowerOn release is done after few clock ticks (2-3).

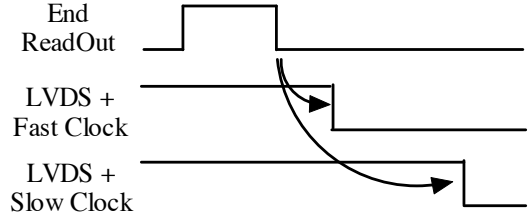


Figure 17: Stop of readout

## IV. PARISROC NEW READOUT

Parisroc [4] integrates a state machine to control the 3 phases: it allows to have a complete autonomous working. Moreover, compare to other ROC chips, it integrates a new channel management: they are completely independent. That's mean, when 1 channel is hit, ADC conversion is started and then the readout of this channel. The readout will only treat hit channels, that's why this module tags each frame with its channel number.

During conversion and readout, acquisition is never stopped: triggers are stacked into SCA and treated as soon as possible (Figure 17).

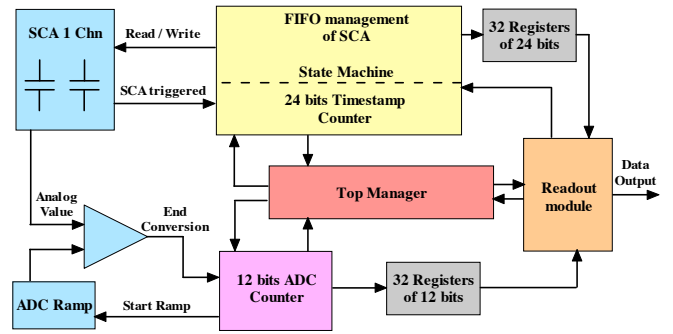


Figure 18: Block diagram

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